VOLTAGE REGULATOR WITH STRESS MODE

FIELD OF THE INVENTION

This invention relates generally to the field of voltage regulators. More particularly, this invention relates to a voltage regulator having both a normal mode and a stress mode to facilitate the testing of voltage regulated devices.

BACKGROUND

Many electronic devices, such as memory chips, are tested using a "burn-in" test. During the burn-in test, the device is operated at an elevated voltage level and temperature. This process will cause marginal devices to fail and results in improved life expectancy for the surviving devices. However, some devices incorporate an internal voltage regulator. If an elevated voltage is supplied to the device, the regulator may be tested but most of the device remains untested because the regulator limits the voltage applied.

SUMMARY

The present invention relates generally to a voltage regulator having a normal mode and a stress mode. Objects and features of the invention will become apparent to those of ordinary skill in the art upon consideration of the following detailed description of the invention.

In one embodiment of the invention a voltage regulator is provided that is operable in a normal mode or a stress mode. In the stress mode, the controlled voltage of the regulator may be elevated to facilitate "burn-in" testing of electronic devices. The stress mode may be invoked, for example, by elevating the voltage supplied to the device above a prescribed maximum operational voltage or by supplying a control signal to the device.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as the preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawing(s), wherein:

FIG. 1 is a diagrammatic representation of an electronic device incorporating voltage regulator in accordance with certain aspects of the present invention.

FIG. 2 is a diagrammatic representation of one embodiment of a voltage divider circuit in accordance with certain aspects of the present invention.

FIG. 3 is a diagrammatic representation of one embodiment of a first voltage follower circuit in accordance with certain aspects of the present invention.

FIG. 4 is a diagrammatic representation of one embodiment of an output circuit in accordance with certain aspects of the present invention.

FIG. 5 is a diagrammatic representation of one embodiment of a second voltage follower circuit in accordance with certain aspects of the present invention.

DETAILED DESCRIPTION

While this invention is susceptible of embodiment in many different forms, there is shown in the drawings and will herein be described in detail one or more specific embodiments, with the understanding that the present disclosure is to be considered as exemplary of the principles of the invention and not intended to limit the invention to the specific embodiments shown and described. In the description below, like reference numerals are used to describe the same, similar or corresponding parts in the several Views of the drawings.

In one embodiment of the invention a voltage regulator is provided that is operable in a normal mode or a stress mode. In the stress mode, the controlled voltage of the regulator may be elevated to facilitate "burn-in" testing of electronic devices. The stress mode may be invoked, for example, by elevating the voltage supplied to the part above a prescribed maximum operational voltage. When the elevated voltage is detected the regulator switches from providing normal voltage level to providing an alternative voltage level. In burn-in testing the alternative voltage level is a higher level. For example, if the normal voltage provided by the regulator is 1.8V, the elevated voltage may be 3.0V. The higher voltage allows the device under test to be stressed during burn-in or other testing. The regulator may alternatively be switched to a stress mode in which the regulated voltage is lower than the normal voltage. This may be useful, for example, for testing the effects of signal degradation. In alternative embodiment, the stress mode is invoked by supplying an external stress-mode control signal to the regulator.

A diagrammatic representation of an electronic device 100 incorporating an exemplary of embodiment of a voltage regulator 101 of the present invention is shown in **FIG. 1**. The regulator is integrated in an electronic device and powers a primary function circuit 134 with interface 136. The primary function circuit performs the primary function of the electronic device, which may be memory storage. In operation, an external voltage signal 102 is applied to a voltage level detector 104. The voltage level detector 104 outputs a stress-mode signal 106 indicative of whether or not the external voltage signal is within a predetermined normal operating range. If the external voltage signal is outside of the predetermined normal operating range, the stress-mode signal causes the regulator to enter a test mode in which the primary function circuit 134 is stressed to reveal faults in the device. In an alternative embodiment, the stress-enable signal is generated external to the device and is supplied to the device by a connector or pin. This avoids the need for the voltage detector circuit 104, but introduces a need for an extra pin on the device and may make the testing of devices more complicated. In the exemplary embodiment shown in **FIG. 1**, the stress-enable signal 106 is coupled to a voltage divider 108 and is used to control the level of an output signal 110 from the voltage divider. The second output 112 of the voltage divider is held at a fixed level. The fixed level is determined by a reference voltage signal 114 from a reference voltage generator 116, which may, for example, be a bandgap voltage generator. The second output 112 of the voltage divider and the reference voltage signal 114 are coupled to the inputs of a first voltage follower 118 that completes a feedback loop and produces

a control signal 120 that controls the voltage divider 108 to maintain the second output 112 at a fixed level relative to the reference voltage signal 114.

The first output signal 110 from the voltage divider is used as a reference voltage for an output stage 122 that provides the regulated voltage signal 124. The regulated voltage signal 124 is used to power the primary function circuit that is integrated with the regulator. The primary circuit may be an array of random access memory cells and associated circuitry, for example. The output stage 122 is controlled by a signal 126 from a second voltage follower circuit 128. The second voltage follower circuit 128 is responsive to the regulated voltage signal 124 and to the first output signal 110 generated by the voltage divider. The voltage follower completes a feedback loop and maintains the regulated voltage signal 124 at the desired level. A bias voltage signal 130 is supplied to the first and second voltage followers. Optionally, a disable signal 132 may be supplied as an input to the second voltage follower 128 to provide a means for disabling the regulator if required.

An exemplary voltage divider 108 is shown in **FIG. 2**. Referring to **FIG. 2**, a supply voltage 202 (labeled VDD) is coupled to ground 204 through a network of elements. Element 206 is a p-channel transistor controlled by the signal 120 from the first voltage follower. The signal 120 is adjusted by the first voltage follower to maintain the voltage level at a first point in the voltage divider at a fixed level. The signal 112 couples the voltage at the first point to an input of the first voltage follower. The next elements in the voltage divider are a resistor 208 in parallel with a p-channel transistor 210. The gate of the transistor 210 receives the stress-enable signal 106. The combined resistance of the transistor 210 and resistor 208 is therefore

controlled by the stress-enable signal. The remaining elements of the divider are additional voltage divider resistors 212 and 214. The output 110 from the voltage divider is used as a reference voltage for the second voltage divider. The level of this reference voltage depends upon the combined resistance of the transistor 210 and resistor 208 is therefore controlled by the stress-enable signal.

An exemplary circuit diagram for the first voltage follower 118 is shown in **FIG. 3**. Referring to **FIG. 3**, the bandgap reference voltage 114 and the reference voltage 112 of the voltage divider are coupled to n-channel transistors 302 and 304, respectively, of a difference amplifier. P-channel transistors 306 and 308 provide an active load to the difference amplifier. The difference amplifier utilizes current mirror (current source) biasing provided by transistors 310 and 312. The biasing level is controlled by the biasing signal 130 that is coupled to the gate of a p-channel transistor 314. Optionally, an additional transistor 316 may be provided for balancing. The output 120 from the first voltage follower is coupled to ground 318 through transistor 320 and capacitor 322.

An exemplary output stage 122 is shown in **FIG. 4**. Referring to **FIG. 4**, a supply voltage 402 is coupled to ground 404 via a p-channel transistor 406 and a capacitor 408. The regulated output voltage signal 124 is passed to the second voltage follower that, in turn, produces control signal 126 that is coupled to the gate of transistor 406. This feedback loop maintains the regulated output voltage signal 124 at the desired level.

An exemplary circuit diagram for the second voltage follower 128 is shown in **FIG. 5**. Referring to **FIG. 5**, the reference voltage 110 from the voltage divider and

the regulated output voltage signal 124 are coupled to n-channel transistors 502 and 504, respectively, of a difference amplifier. P-channel transistors 506 and 508 provide an active load to the difference amplifier. The difference amplifier utilizes current mirror (current source) biasing provided by transistors 510 and 512. The biasing level is controlled by the biasing signal 130 that is coupled to the gate of a p-channel transistor 514. Optionally, transistors 516 and 518 may be included. The gate transistor 518 is controlled by signal 520 that is asserted when the regulator is active. The output 126 may be coupled to the voltage supply 522 through p-channel transistor 524 by passing the disable signal 132 through an inverter 526 to the gate of the transistor 524. The signal 126 is supplied to the gate of a p-channel transistor (406 in **FIG. 4**) and so asserting this signal disables the regulated output voltage signal (124 in **FIG. 4**). The disable signal also disables the difference amplifier by shorting the amplifier bias signal 528 to ground via n-channel transistor 530.

While the invention has been described in conjunction with specific embodiments, it is evident that many alternatives, modifications, permutations and variations will become apparent to those of ordinary skill in the art in light of the foregoing description. Accordingly, it is intended that the present invention embrace all such alternatives, modifications and variations as fall within the scope of the appended claims.